INAF Technical Report

LRS: Implementation of ARC controller

Document version 2.2

TNG-DD-LRS-0001

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Rosario Cosentino

INAF – Osservatorio Astrofisico di Catania

Fundación Galileo Galilei (TNG)

With the technical support of:

Marcos Hernandez Diaz

Fundación Galileo Galilei (TNG)

Change Record

Issue/Rev.	Date	Section/Page affected	Reason/Remarks
V1.0		First version	draft
V1.1	13/07/2018		
V2.0	03/08/2018	Added the LRS connections	
V2.1	20/08/2018	Added LRS settings	
V2.2	27/3/2020	Changes in clock cable	

Contents

1. Introduction

1.1 Scope

This document is intended to give all the information about the operations to be done for the upgrade of the existing cryostat to the new acquisition system based on the ARC controller. This documentation includes the internal wiring and the cables specifications.

1.2 Contact information

Feedback on this document is encouraged. Please email to cosentino@tng.iac.es

1.3 Reference documents

[RD01] **E2V datasheet: CCD42-40 Back Illuminated High Performance CCD sensor**

[RD02] **TNG-DD-CCD-0001_Preamplifier-mount**

[RD03] **TNG-DD-CCD-0002_Clock-board-mount**

[RD04] **TNG-RS-LRS-0002, LRS: ARC Software Specification Description**

2. The CCD mounting

2.1 The CCD detectors

FEATURES

- 2048 by 2048 pixel format
- 13.5 µm square pixels
- Image area 27.6 x 27.6 mm
- Back Illuminated format for high quantum efficiency
- Full-frame operation
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Dual responsivity output amplifiers
- Wide dynamic range for 15-bit operation
- Gated dump drain on output register
- 100% active area
- New compact footprint package

APPLICATIONS

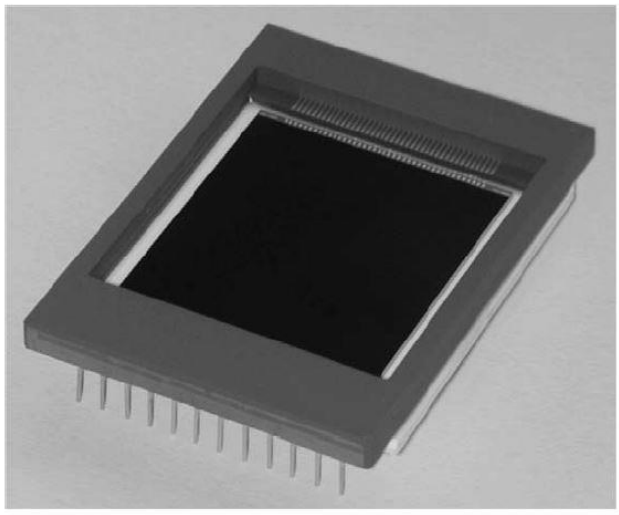


Figure 1 - E2V 4240 CCD

2.2 The cryostat wiring

2.2.1 Heater and temperature sensors

In the rear side of the cold finger are connected the braided cables, the heater and the temperature sensors

The detectors have been mounted by using the M83513 and MWDM2L-21SS connectors (see appendix). The temperature telemetry and control was done by using a Lakeshore 331 controller and two PT100 sensors. The wiring is shown in Table 1 and in Figure 2.

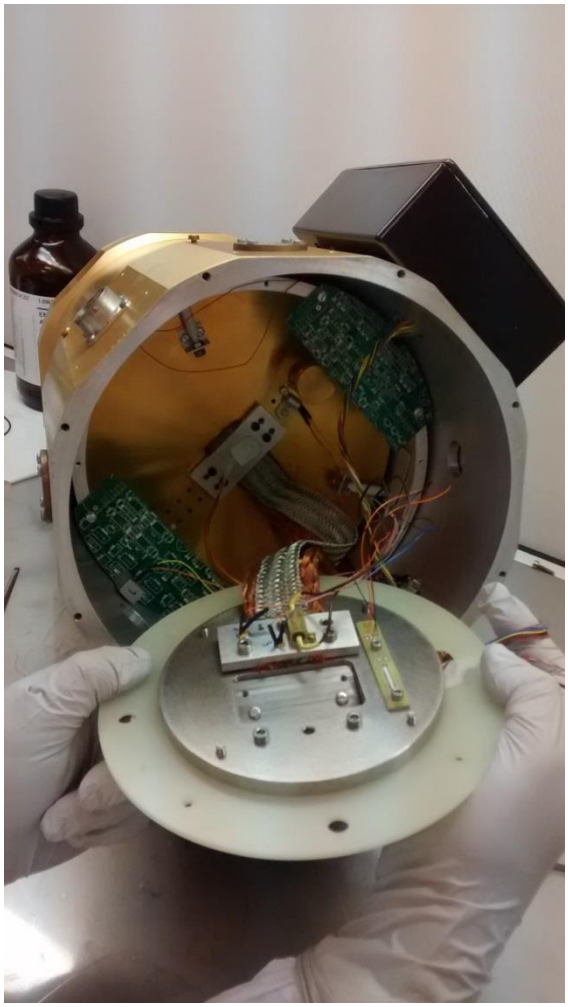


Table 1 - Wiring of temperature control

Connettore Cryostat	Connessioni cryostat		
DT02H-16-26PN	Signal	sensor	Color
H	Heater	resistor	
J	Heater	resistor	
K	Cold finger	PT100	black
L	Cold finger	PT100	black
M	NL2	PT100	orange
N	NL2	PT100	black
P	NL2	PT100	orange
R	NL2	PT100	black
Y	Cold finger	PT100	orange
Z	Cold finger	PT100	orange

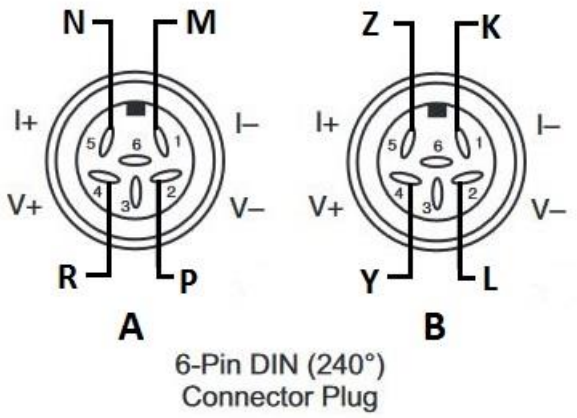


Figure 2 - Lakeshore 311 pinout

2.2.2 The Cloks Signals

Supporto per CCD42-40-5-102 (CCD per Dolores Deep Depletion Grado 5)
Connessioni per le linee di clock Connettore J1

CCD Pin Number	Function	Pcb Strip	26 Pin Cryo Connector	CCD Controller Connector Pin Number	CCD Contr. 44 Pin Connector Function
	DGND	16	A		
	DGND	15	A	22	
	DGND	14	A		
7	DUMP GATE	13	D	36	OVPH3A
	DGND	12	A		
14	θR	11	H	12	OHPH6
15	SW	10	F	29	OHPH5
16	Iθ3	9	G	35	OVPH2A
17	Iθ1	8	J	17	OVPH0A
18	Iθ2	7	K	31	OVPH1A
19	Rθ2L	6	N	16	OHPH1
20	Rθ1L	5	L	15	OHPH0
21	Rθ3	4	M	14	OHPH2
22	Rθ1R	3	P	30	OHPH3
23	Rθ2R	2	R	13	OHPH4
	DGND	1	A		

Il clock verticale V3A tramite Jumper e' utilizzato per il Dump Gate Attualmente il viene pilotato a –2 Volt.
Esiste un solo contatto di massa nel pin A del connettore da vuoto.

Figure 3 - original documentation of the clocks cabling

Table 2 - Pinout and clock connections

Cryostat Connector	Clock filter				CCD Board		Used
62GB-16F16-26SN	Clock	Segnale	C.colors	board	CCD:Pin:conn	Color	
A		GND					
B		NC					
C		NC					
D	V4	I01-B		J5-12	7		
E		NC					
F	H6	SW		J2-6	15		
G	V3	I03-A		J5-11	16		
H	H7	0R-LR		J2-7	14		
J	V1	I01-A		J5-9	17		
K	V2	I02-A		J5-10	18		
L	H1	R01L		J2-1	20		
M	H3	R03-A		J2-3	21		
N	H2	R02L		J2-2	19		
P	H4	R01R		J2-4	22		
R	H5	R02R		J2-5	23		
S							
T							
U							
V							
W							
X							
Y							
Z							
a							
b-c	NOT USED						

Figure 4 - LRS Clock wiring

2.2.3 Pinout and Bias connection

Supporto per CCD42-40-5-102 (CCD per Dolores Deep Depletion Grado 5)
Connessioni per Video Linee e Bias

CCD Pin Number	Function	Pcb Strip	26 Pin Cryo Connector	CCD Controller Connector Pin Number	CCD Contr. 44 Pin Connector Function
	GND (RET)	1	G		
3	VOSL	2	H	17	+VIDEO_IN3
	V1ODL	3		2	-VIDEO_IN3
1-12-13-24	SS	4	D	35	VB5
2	OG1	5	Y	39	VB9
4	ODL	6	A	31	VB1
5	RDL	7	M	32	VB2
6	DD	8	N	34	VB4
	GND	9	F	26,23,8,24,11, 27,9,25,10	AGND PREAMP AGND
7	DG		Vedi Clock		
8	RDR	10	R	33	VB3
	ODL	11			VB1
9	ODR	12	A	31	VB1
11	OG2	13	B	40	VB10
	V1ODR	14			
				44	Clamp
10	OSR	15	J	16	+VIDEO_IN4
	GND (RET)	16	K	1	-VIDEO_IN4

Le due video linee VOSL e VOSR (sulla PCB e' riportatoOSR per errore) NON hanno carico sulla basetta di supporto del chip e sono twistate con un filo di GND. Tutte le tensioni di bias sono filtrate con 6.8μF elettrolitici piu' 0.1μF non polarizzate piu' una resistenza da 10Ω. Le Tensioni di Drain ODR/ODL sono in comune. Per quanto riguarda il DG (Dump gate pin 7 CCD) esso potra' essere collegato ad una fase verticale V3A proveniente dalla strip clock oppure a GND proveniente dalle fasi oppure a AGND proveniente dalla CDS tramite uno jumper schematizzato di seguito. Nel nostro caso utilizzeremo DG sempre a GND. GND e' il round locale alla basetta e separato dal round digitale.

Figure 5 - Original documentation of video line and bias

Table 3 - Pinout and connections of bias and video

Cryostat Connector	Preamplifier				CCD Board		Used
62GB-16F16-26SN	Signal (value)	board	Signal	C.colors	CCD:Pin:conn	Color	
A	Bias 1 (27 V)	J8-1	ODL-R		4 and 9		YES
B	Bias 10 (2 V)	J8-10	OG2		11		YES
C							NO
D	Bias 5 (7 V)	J8-5	SS		1-12-13-24		YES
E							NO
F			GND				YES
G			GND-RET				YES
H	Video 3 - pos	Vin1-1	VOSL		3		YES
J	Video 4 - pos.	Vin1-2	OSR		10		YES
K			GND-RET				YES
L							NO
M	Bias 2 (15 V)	J8-2	RDL		5		YES
N	Bias 4 (22 V)	J8-4	DD		6		YES
P							NO
R	Bias 3 (15 V)	J8-3	RDR		8		YES
S							NO
T							NO
U							NO
V							NO
W							NO
X							NO
Y	Bias 9 (1 V)	J8-9	OG1		2		YES
Z							
a							
b							
c							

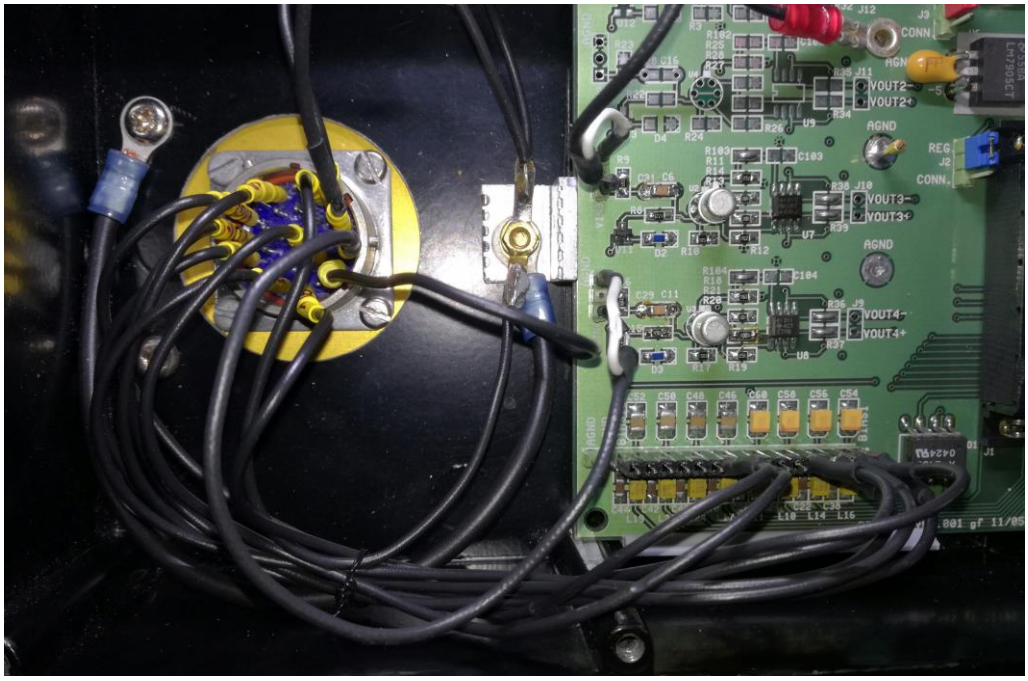


Figure 6 - LRS bias connections

2.2.4 Clocks and Bias voltages

The following table shows the values of current CCD settings, the values used in the instrument are the "Set Volt" column and correspond to the table values of Skytech configuration file.

Volori dei Bias e dei clock con offset					
Bias	Default VOLT	Offset VOLT	Set VOLT		
ODL(VB1)	29	2	27	Bias 1	
RDL(VB2)	17		15	Bias 2	
RDR(VB3)	17		15	Bias 3	
DD(VB4)	24		22	Bias 4	
SS(VB5)	9		7	Bias 5	
OG1(VB9)	3		1	Bias 9	
OG2(VB10)	4		2	Bias 10	
DUMP Gate	0		-2	Clock V4	
CLOCK Lines	Offset VOLT	Default VOLT NEG	Default VOLT POS	Set VOLT NEG	Set VOLT POS
H0(R01L)	2	1	11	-1	9
H1(R02L)		1	11	-1	9
H2(R03)		1	11	-1	9
H3(R01R)		1	11	-1	9
H4(R02R)		1	11	-1	9
H5(SW)		1	11	-1	9
H6(Reset)		0	12	-2	10
V0A(I01)		0	10	-2	8
V1A(I02)		0	10	-2	8
V2A(I03)		0	10	-2	8

Figure 7 - LRS values of current settings

2.2.5 The CCD board

The detector was been connected by using the custom CCD board (see Figure 8). In Table 2 and Table 3 the details of the internal connections between the vacuum connectors MIL-16-26 and the clock and video-bias boxes are shown.

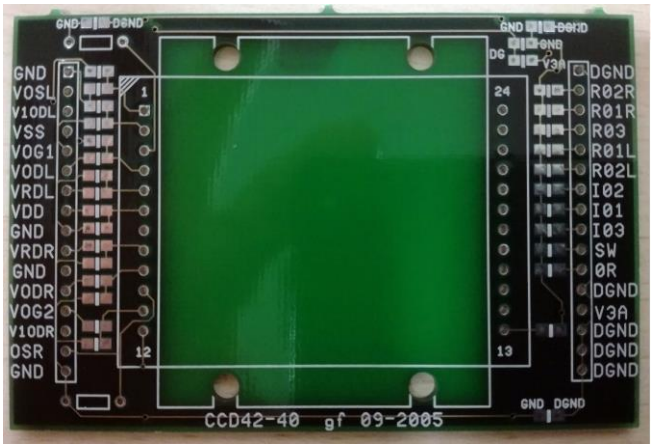


Figure 8 - CCD board

2.3 The Clock and Video-Bias Boxes

The two boxes containing the clock and video-bias boards are connected to the cryostat, very close to the CCD, to increase EMC and avoid EMI.

The clock board provides a passive filter of clocks signals; the video-bias contains a passive filter of the CCD bias voltages and a four channels preamplifier for the CCD video lines.

The details of these boxes, the mounting procedure of clock and Video-bias boards and the list of components (BOM) are specified in [RD02] and in [RD03].

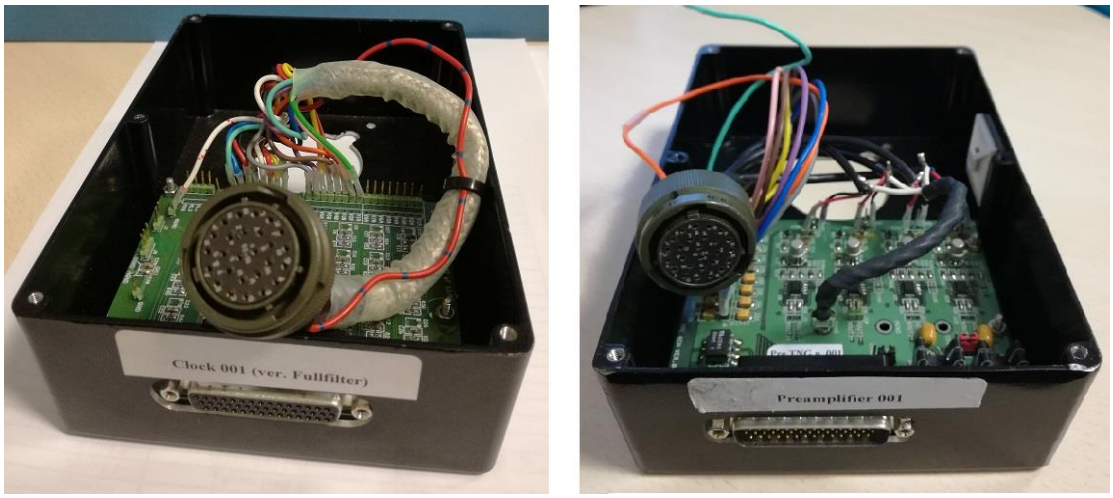


Figure 9 - The clock and Video-Bias Boxes

3. The ARC controller

The ARC controller is provided by astronomical research camera l.t.d. together with the drivers and a template software. The cabling, connectors, preamplifier and assembler code to drive and read the CCD detectors has to be developed by the user [RD04].

In the following paragraphs, we describe the connections from the ARC board to the panel of the CCD controller and the cables that connect the ARC controller to the detectors taking into account the possibility of use the preamplifier or a direct connection with the CCD.

For this reason, we had foreseen two cables, named option 1 and option2.

In Figure 10 and in Figure 11 the layouts of these two options are shown.

The connector's characteristics, the serial number and the distributors can be found in Appendix A.

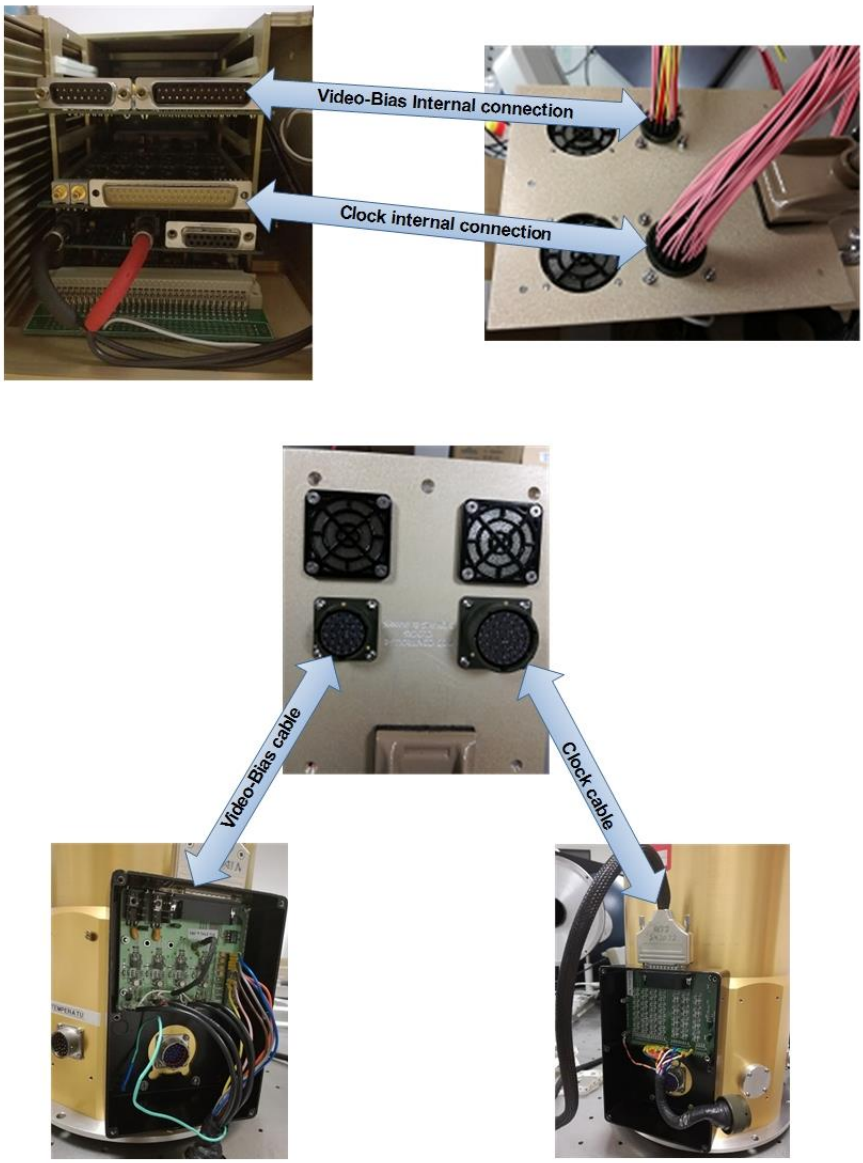


Figure 10 - ARC internal wiring and option 1 connections cable

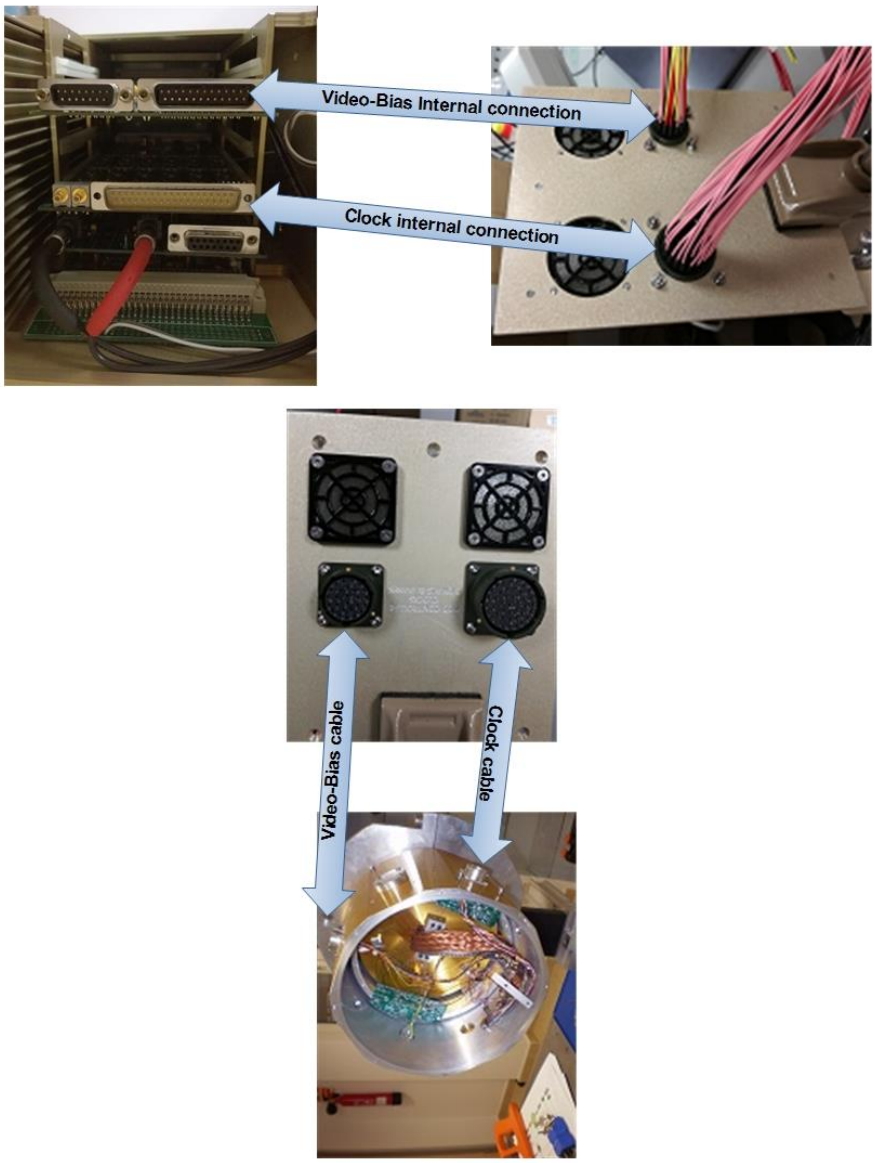


Figure 11 - ARC internal wiring and option 2 connections cables

3.1 ARC internal wiring

The ARC controller boards provide the bias voltages and the clocks sequences through two DB connectors (DB-25 and DB-37) and use a DB-15 connector for the video signal and power supply. The ARC case front panel has to be machined to mount the MIL connectors and then the wiring between the DB and MIL connectors has to be done. In Figure 10 and Figure 11 are shown the pictures of the internal wiring and the panel mechanization, in Table 4 and Table 5 are shown the details of the wirings.

In Appendix A the details of the connectors, including type, manufacturer serial number, distributor serial number and a short description are shown.

Table 4 - Video-Bias ARC internal connections

CCD Controller ARC			Signal name
DB-25	DB-15	MIL 16-26	
FCE17-B25SM-240	FCE17-A15SM-240	62GB-12E16-26SN	
1		A	Bias 1
2		B	Bias 2
3		C	Bias 5
4		D	Bias 6
5		E	Bias 3
6		F	Bias 4
7		L	GND
8		U	GND
9		W	Bias 13
10		X	Bias 14
14		T	-15 VA
15		S	+15 VA
16		Z	-6 VA
17		b	+6VA
	1	G	Single ended input CH A
	2	c	Video 1 - pos.
	3	H	Video 1 - neg.
	6	N	Video 3 - neg.
	7	a	Video 3 - pos.
	8	M	Single ended input CH B
	9	Y	GND
	12	v	GND
DB-37 pin 11		P	clamp
		R	
		J	
		K	

Table 5 - Clock ARC internal connections

CCD Controller ARC			
DB-37	**MIL 20-41**	**SIGNAL**	**Note**
DC-37S-A191-A197	**62GB-12E20-41SN**		
1	J	CLK0	Reset Gate Left
2	b	CLK1	Reset Gate Right
3	A	CLK2	Serial #1 Left
4	E	CLK3	Serial #1 Right
5	B	CLK4	Serial #2 Left
6	F	CLK5	Serial #2 Right
7	D	CLK6	Serial #3 Both
8	G	CLK7	Summing Well Left
9	c	CLK8	Summing Well Right
10	K	CLK9	Dump Gate (NO)
13	L	CLK12	I1
14	M	CLK13	I2
15	P	CLK14	I3
16	R	CLK15	Dump Gate
17	S	CLK16	Unused
18	a	CLK17	Unused
19	Y	CLK18	Unused
22	C	GND	GND
23	H	GND	GND
24	N	GND	GND
25	U	GND	GND
26	V	GND	GND
27	W	GND	GND
28	Z	GND	GND
29	T	GND	GND
33	X	CLK19	
11	Mil 16-26 pin P	clamp	
30	d	GND	
31	shell	GND	

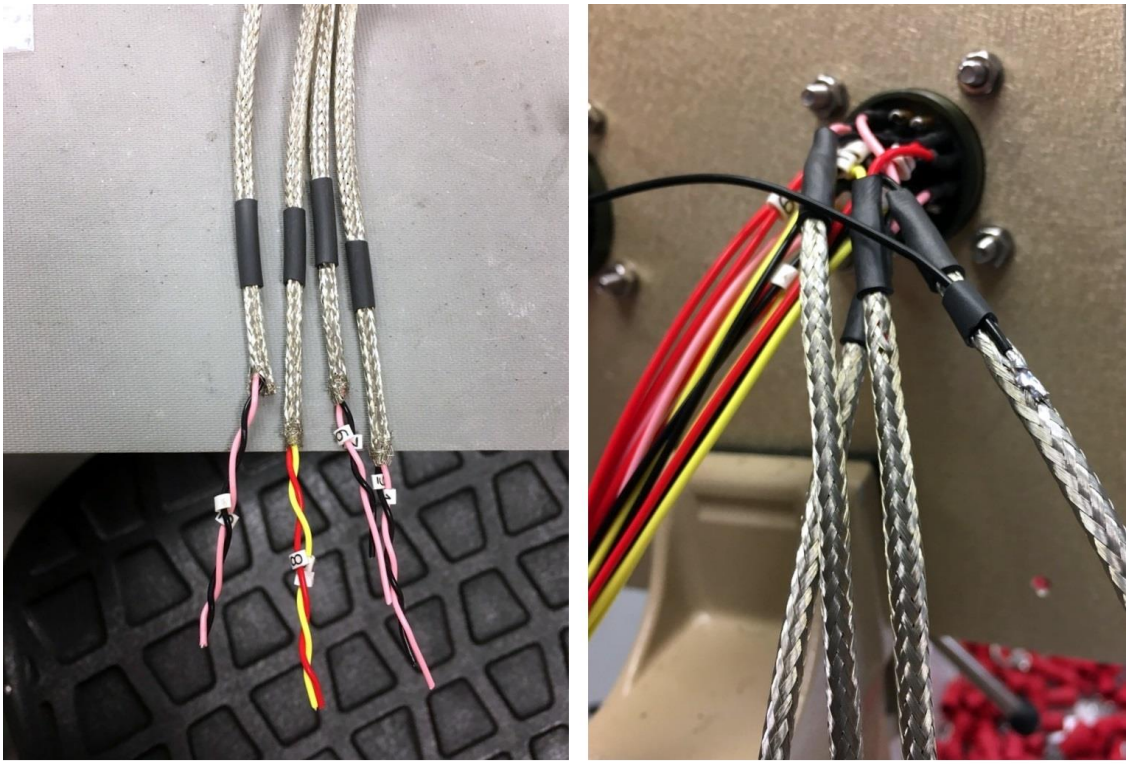


Figure 12 - ARC internal video-bias connections with a detail of video signals (shielded)

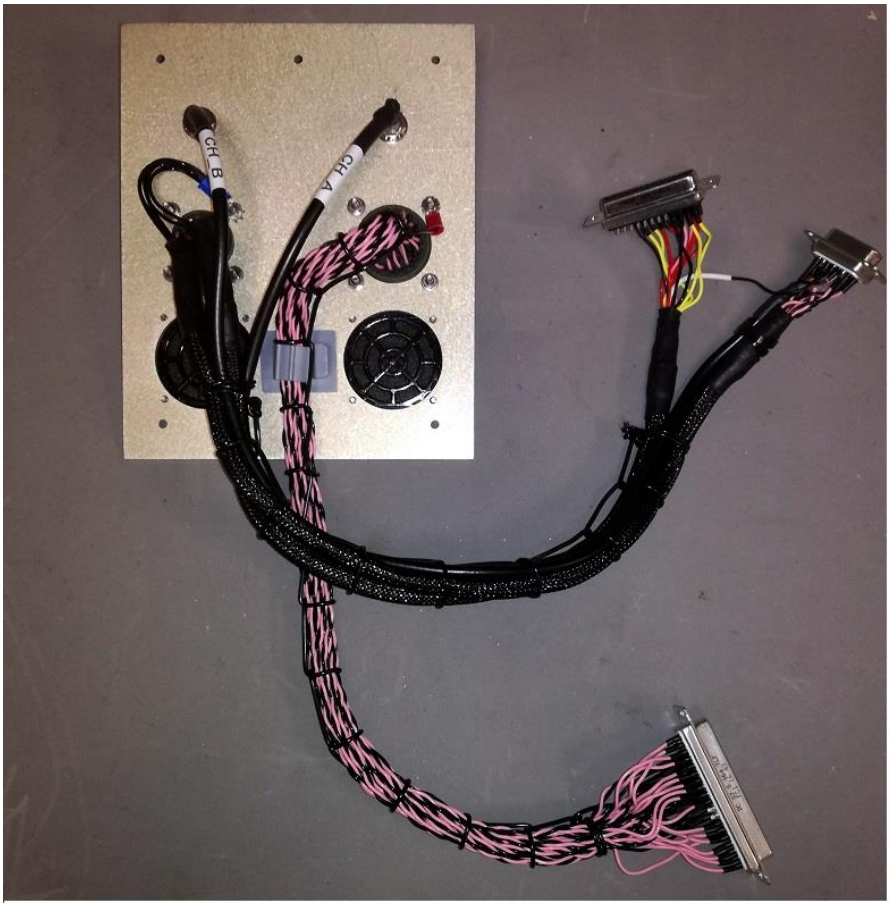


Figure 13 - ARC internal connections (Video-Bias and Clocks)

3.2 The Clocks and Video-Bias cables (Option 1)

In this option (shown in Figure 10) we had foreseen the use of a preamplifier for the video signal and passive filter for the clock sequences. This means that we have to manufacturer the cables from the CCD controller to the clocks and preamplifier boards. In Table 6 and Table 7 are shown the details of the cables, including the connector's serial code and the distributor code of the wires.

In Appendix A the details of the connectors, including type, manufacturer serial number, distributor serial number and a short description are shown.

Table 6 - ARC controller to Preamplifier box cable

MIL 16-26	DB-44 (female)	wire	Colors	Signal name
62GB-56T16-26PN	L77HDB44S			
R	1	Farnell 860160	Negro	Video 4 - neg.
N	2	Farnell 860160	Negro	Video 3 - neg.
K	3	Farnell 860160	Negro	Video 2 - neg.
H	4	Farnell 860160	Negro	Video 1 - neg.
	5	Farnell 860160		Comm.Video Shield
Z	6			-6 VA
T	7	Yes		-15 VA
V	8			GND
L	9			GND
U	10	Shield*		GND
G	19	Farnell 860160	Negro	Single ended input CH A
M	17	Farnell 860160	Negro	Single ended input CH B
P	16	Farnell 860160	Rojo	Video 4 - pos.
a	17	Farnell 860160	Rojo	Video 3 - pos.
J	18	Farnell 860160	Rojo	Video 2 - pos.
c	19	Farnell 860160	Rojo	Video 1 - pos.
Y	20			GND
b	21			+6VA
S	22			+15 VA
X	29	RS 482-5730	Verde/Rojo	Bias 14
A	31	RS 482-5730	Rojo	Bias 1
B	32	RS 482-5730	Azul	Bias 2
E	33	RS 482-5730	Verde	Bias 3
F	34	RS 482-5730	Amarillo	Bias 4
C	35	RS 482-5730	Blanco	Bias 5
D	36	RS 482-5730	Negro	Bias 6
W	43	RS 482-5730	Rojo/Azul	Bias 13

Table 7 - ARC controller to clock box cable

MIL 20-41	DB-44 (male)	Signal	Note
62GB-585-20-41P	L717HDB44P		
J	12	OHPH6	Reset Gate Left
b	2	changed	Reset Gate Right
A	15	OHPH0	Serial #1 Left
E	30	OHPH3	Serial #1 Right
B	16	OHPH1	Serial #2 Left
F	13	OHPH4	Serial #2 Right
D	14	OHPH2	Serial #3 Both
G	29	OHPH5	Summing Well Left
c	3	changed	Summing Well Right
K	28	OHPH7	Dump Gate
L	32	OVPH0B	I1
M	33	OVPH1B	I2
P	34	OVPH2B	I3
R	37	OVPH3B	Unused
S	21	OVPH4B	Unused
a	20	OVPH5B	Unused
Y	19	OVPH6B	Unused
C	5	GND	GND
H	6	GND	GND
N	N.C.		GND
U	N.C.		GND
V	N.C.		GND
W	N.C.		GND
Z	22	GND	GND
T	23	GND	GND
X	1	OVPH7B	

Figure 14 - Clock and Video-Bias cables (option 1)

3.3 The Clocks and Video-Bias cables (Option 2)

In this option (shown in Figure 11) we had foreseen the direct connection of the CCD to the ARC controller or the use of new dedicated preamplifier and clock board. This means that we have to manufacturer the cables from the CCD controller to the cryostat. In Table 8 and Table 9 are shown the details of the cables, including the connector's serial code and the distributor code of the wires.

In Appendix A the details of the connectors, including type, manufacturer serial number, distributor serial number and a short description are shown.

Table 8 - ARC controller to CCD cable (Video-Bias)

MIL 16-26	MIL 16-26	Cable	Colors	Signal name
62GB-56T16-26PN				
R	R	Farnell 860160	Negro	Video 4 - neg.
N		Farnell 860160	Negro	Video 3 - neg.
K	K	Farnell 860160	Negro	Video 2 - neg.
H		Farnell 860160	Negro	Video 1 - neg.
		Farnell 860160		Comm.Video Shield
Z	Z			-6 VA
T	T	Yes		-15 VA
v	v			GND
L	L			GND
U	U	Shield*		GND
G	G	Farnell 860160	Negro	Single ended input CH A
M	M	Farnell 860160	Negro	Single ended input CH B
P	P	Farnell 860160	Rojo	Video 4 - pos.
a	a	Farnell 860160	Rojo	Video 3 - pos.
J	J	Farnell 860160	Rojo	Video 2 - pos.
c		Farnell 860160	Rojo	Video 1 - pos.
Y	Y			GND
b	b			+6VA
S	S	Yes		+15 VA
X	X	RS 482-5730	Verde/Rojo	Bias 14
A	A	RS 482-5730	Rojo	Bias 1
B	B	RS 482-5730	Azul	Bias 2
E	E	RS 482-5730	Verde	Bias 3
F	F	RS 482-5730	Amarillo	Bias 4
C	C	RS 482-5730	Blanco	Bias 5
D	D	RS 482-5730	Negro	Bias 6
W	W	RS 482-5730	Rojo/Azul	Bias 13

Table 9 - ARC controller to CCD cable (clocks)

MIL 20-41 62GB-585-20-41P	MIL 16-26 62GB-56T16-26PN	Signal	Note
J	J	OHPH6	Reset Gate Left
b	b	changed	Reset Gate Right
A	A	OHPH0	Serial #1 Left
E	E	OHPH3	Serial #1 Right
B	B	OHPH1	Serial #2 Left
F	F	OHPH4	Serial #2 Right
D	D	OHPH2	Serial #3 Both
G	G	OHPH5	Summing Well Left
c	c	changed	Summing Well Right
K	K	OHPH7	Dump Gate
L	L	OVPH0B	I1
M	M	OVPH1B	I2
P	P	OVPH2B	I3
R	R	OVPH3B	Unused
S	S	OVPH4B	Unused
a	a	OVPH5B	Unused
Y	Y	OVPH6B	Unused
C	C	GND	GND
H	H	GND	GND
N	N		GND
U	U		GND
V	V		GND
W	W		GND
Z	Z	GND	GND
T	T	GND	GND
X	X	OVPH7B	

4. Clocks and Bias configuration

In this chapter are described the settings for the e2v 42-40 taking into account the e2v datasheet and the different architecture of the two CCD controller that we are using at TNG.

The first part is dedicated to an overview of the typical settings suggested by e2v and are shown the timing of the datasheet.

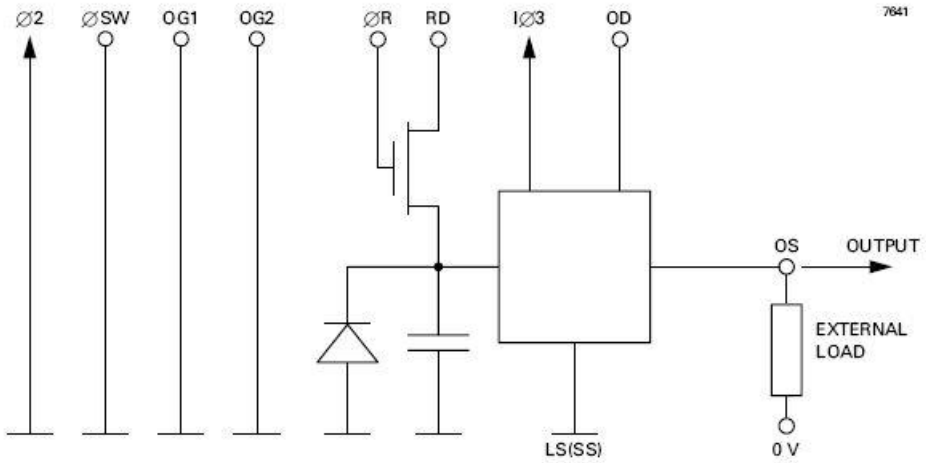
The following paragraph describe the implementation of the CCD e2v 42-40 with the skytech controller, including the configuration files and the output of the clocks sequences and the bias values as generated by the CCD controller.

The last paragraph shows the implementation of the CCD with the ARC controller.

4.1 Settings of CCD E2V 42-40

Ref	Pin No.	Typical Voltage	Note
SS	1, 12, 13, 24	9.5 V	
I11	17	12 V	
I12	18	12 V	
I13	16	12 V	
R11(L)	20	11 V	
R12(L)	19	11 V	
R11(R)	22	11 V	
R12(R)	23	11 V	
R13	21	11 V	
1R	14	12 V	
1SW	15	11 V	
DG	7	0 V	Non-charge dumping level is shown. For charge dumping, DG should be pulsed to 12 + 2 V.
OG1	2	3 V	
DD	6	24 V	
OG2	11	see note 7	OG2= OG1+1 V - normal low noise mode or OG2=20 V - low responsivity/increased charge handling mode.
OD(L)	4	29 V	
OD(R)	9	29 V	
OS(L)	3	see note 8	OS = 3 to 5 V below OD typically. Use 3 – 5 mA current source or 5 – 10 kW load.
OS(R)	10	see note 8	OS = 3 to 5 V below OD typically. Use 3 – 5 mA current source or 5 – 10 kW load.
RD(L)	5	17 V	
RD(R)	8	17 V	

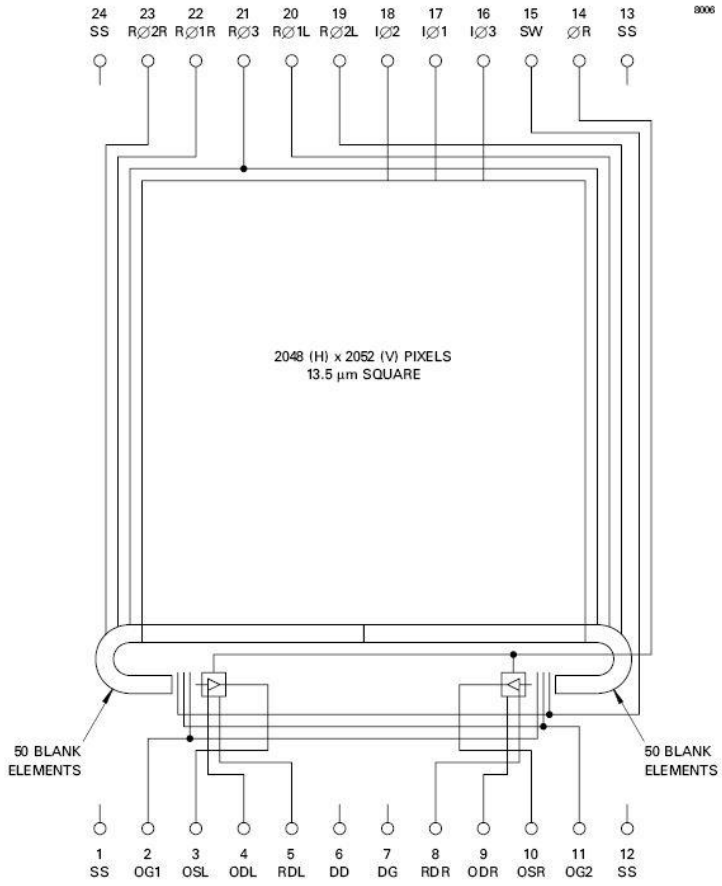
OUTPUT CIRCUIT



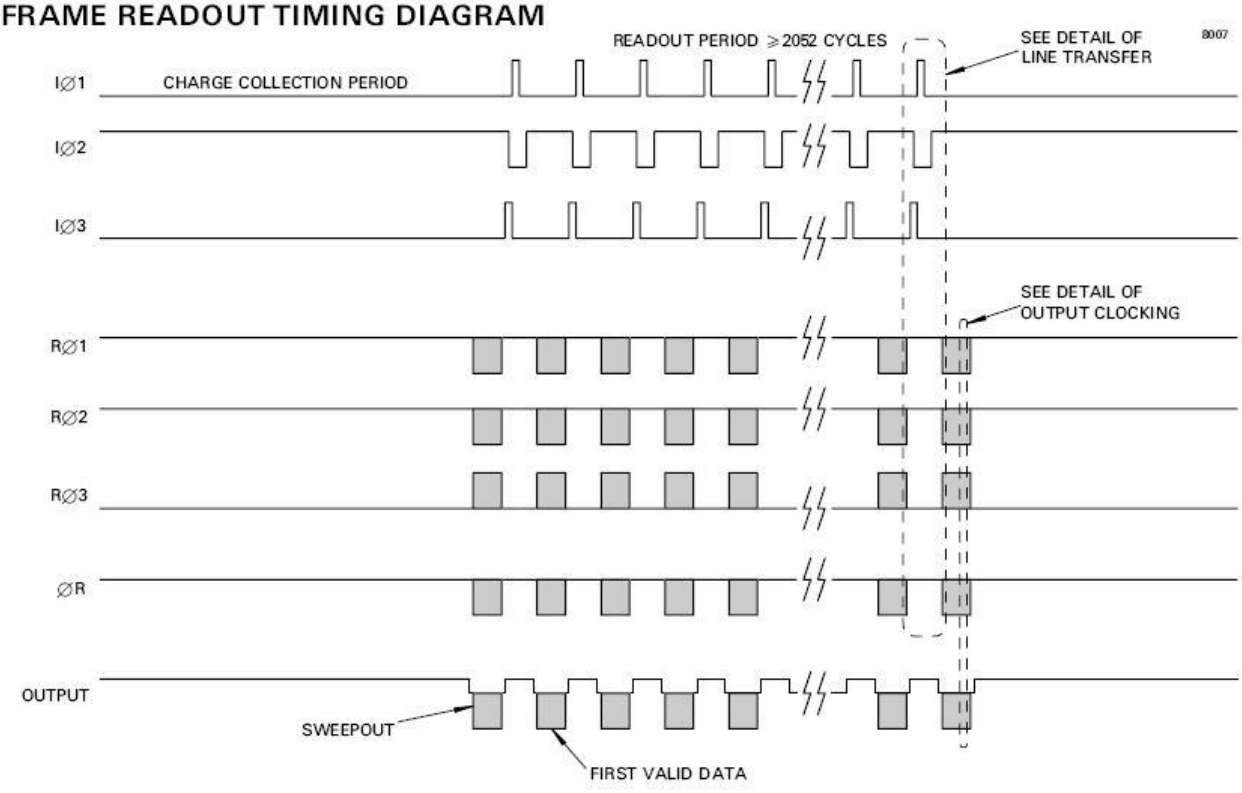
CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK LOW	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS
			Typical	Min	Typical	Max	with respect to V_{SS}
1	SS	Substrate	n/a	0	9	10	-
2	OG1	Output gate 1	n/a	2	3	4	±20 V
3	OSL	Output transistor source (left)	n/a		see note 9		−0.3 to +25 V
4	ODL	Output drain (left)	n/a	27	29	31	−0.3 to +25 V
5	RDL	Reset drain (left)	n/a	15	17	19	−0.3 to +25 V
6	DD	Dump drain	n/a	22	24	26	−0.3 to +25 V
7	DG	Dump gate (see note 10)	0	-	12	15	±20 V
8	RDR	Reset drain (right)	n/a	15	17	19	−0.3 to +25 V
9	ODR	Output drain (right)	n/a	27	29	31	−0.3 to +25 V
10	OSR	Output transistor source (right)	n/a		see note 9		−0.3 to +25 V
11	OG2	Output gate 2 (see note 11)	4	16	20	24	±20 V
12	SS	Substrate	n/a	0	9	10	-
13	SS	Substrate	n/a	0	9	10	-
14	∅R	Reset gate	0	8	12	15	±20 V
15	SW	Summing well			Clock as R∅3		±20 V
16	I∅3	Image area clock, phase 3	0	8	10	15	±20 V
17	I∅1	Image area clock, phase 1	0	8	10	15	±20 V
18	I∅2	Image area clock, phase 2	0	8	10	15	±20 V
19	R∅2L	Register clock phase 2 (left)	1	8	11	15	±20 V
20	R∅1L	Register clock phase 1 (left)	1	8	11	15	±20 V
21	R∅3	Register clock phase 3	1	8	11	15	±20 V
22	R∅1R	Register clock phase 1 (right)	1	8	11	15	±20 V
23	R∅2R	Register clock phase 2 (right)	1	8	11	15	±20 V
24	SS	Substrate	n/a	0	9	10	-

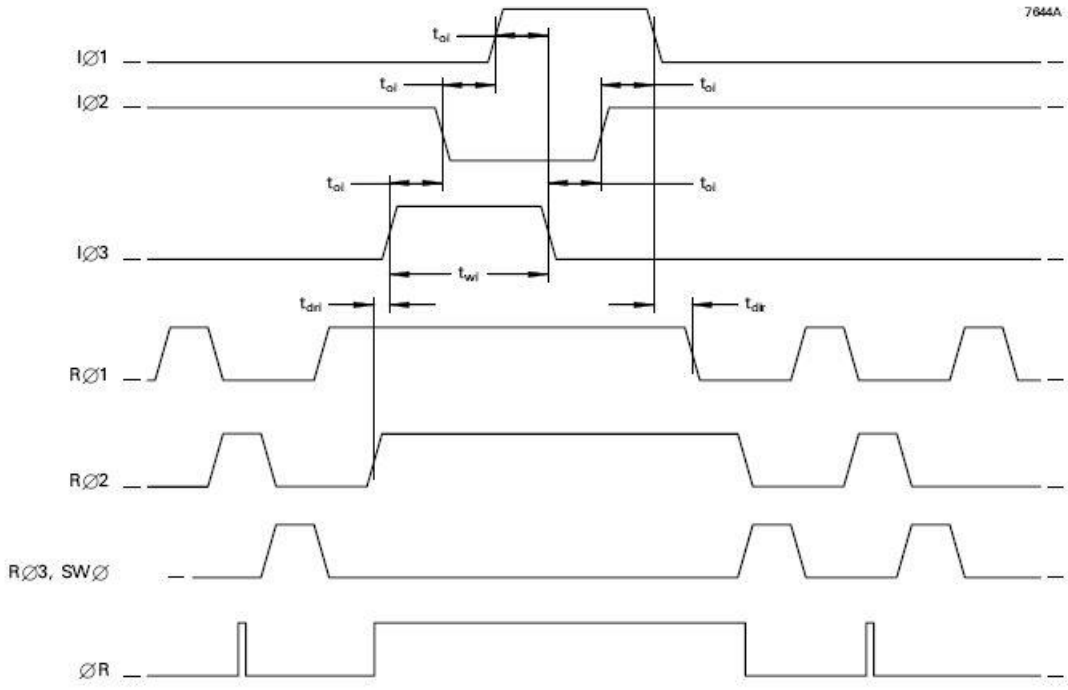
DEVICE SCHEMATIC



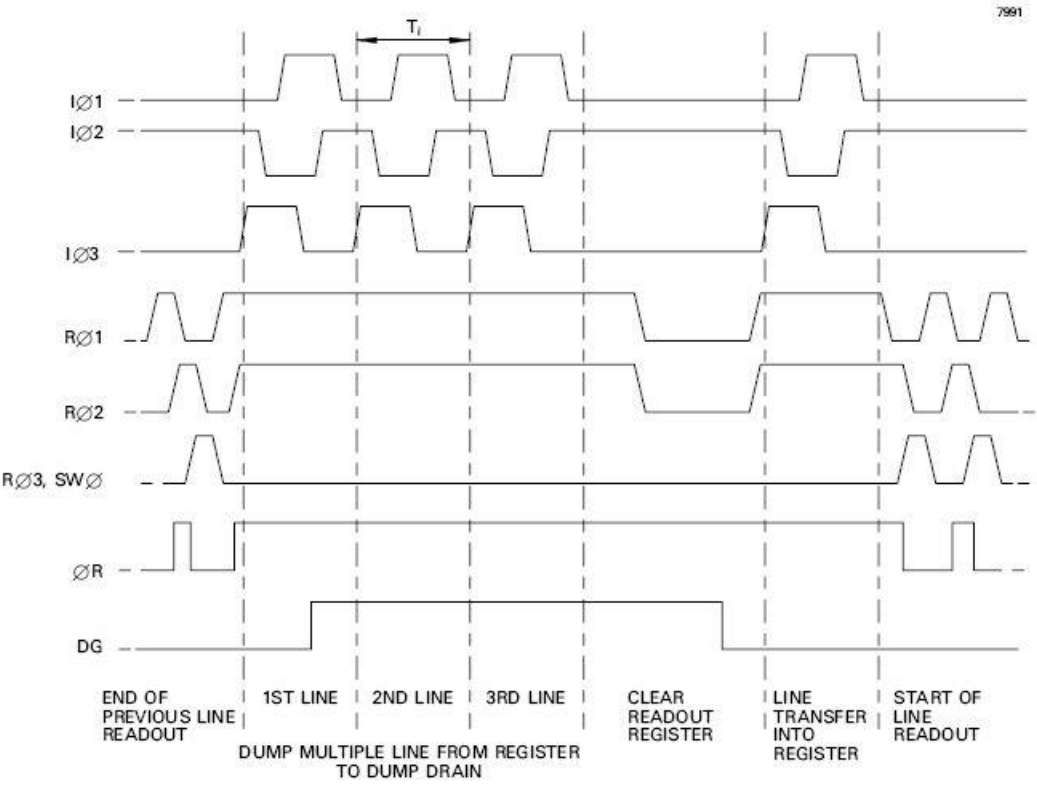
FRAME READOUT TIMING DIAGRAM



DETAIL OF LINE TRANSFER (Not to scale)



DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



4.2 Clocks configuration for the Skytech controller

In this paragraph are reported the voltage values of the Vertical and Horizontal clocks, for the low and high levels and the assignment to the CCD phases (Table 10).

The figures from Figure 15 to Figure 21 show the waveform used for the different readout modes allowed by the CCD control system based on the Skytech controller.

Table 10 - LRS settings of the Skytech controller

#	Horizontal H	Horizontal L	Signal
1	9	-1	I01
2	9	-1	I02
3	9	-1	I03
4	9	-1	DG
5	9	-1	
6	9	-1	
7	10	-2	
8	8	-2	

#	Vertical H	Vertical L	Signal
1	8	-2	R01L
2	8	-2	R02L
3	8	-2	R03
4	8	-2	R01R
5	8	-2	R02R
6	8	-2	SWLR
7	8	-2	RG
8	8	-2	STC

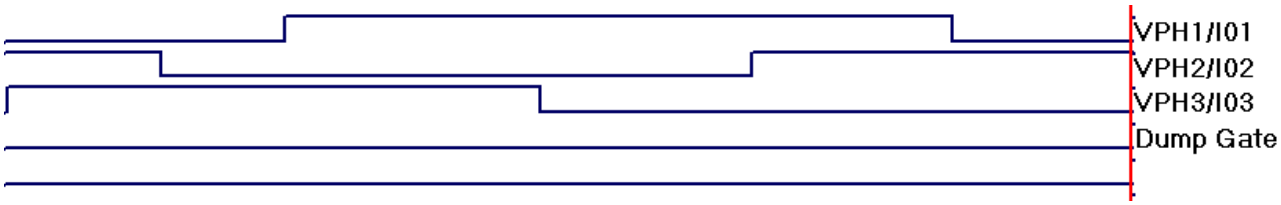


Figure 15 - Vertical phases

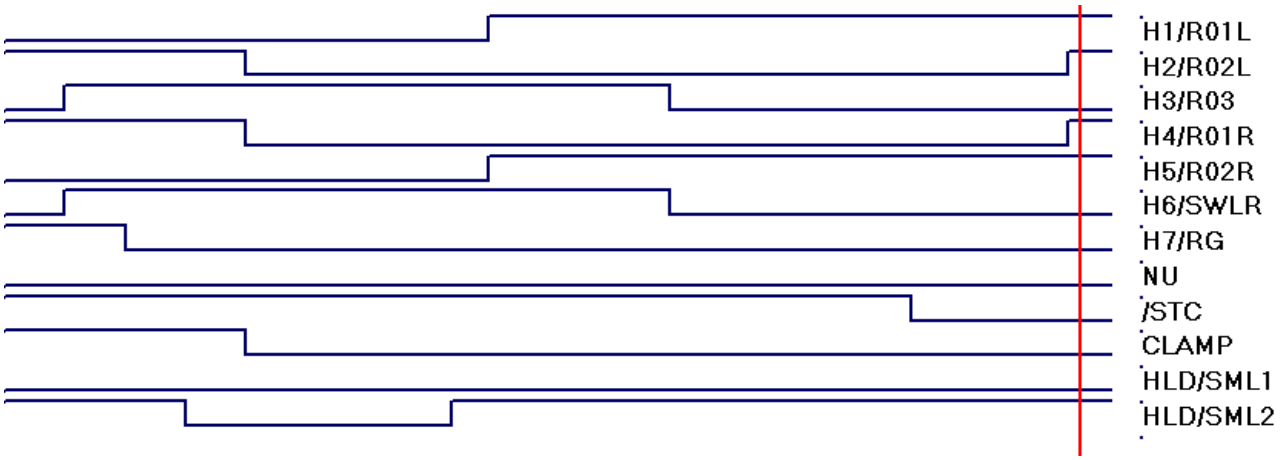


Figure 16 - Horizontal readout right

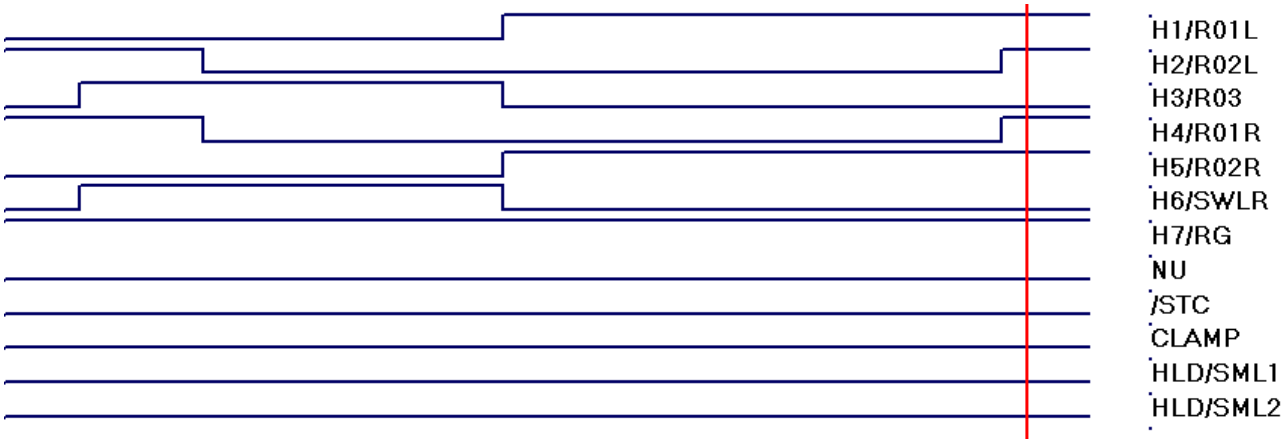


Figure 17 - Horizontal skip right

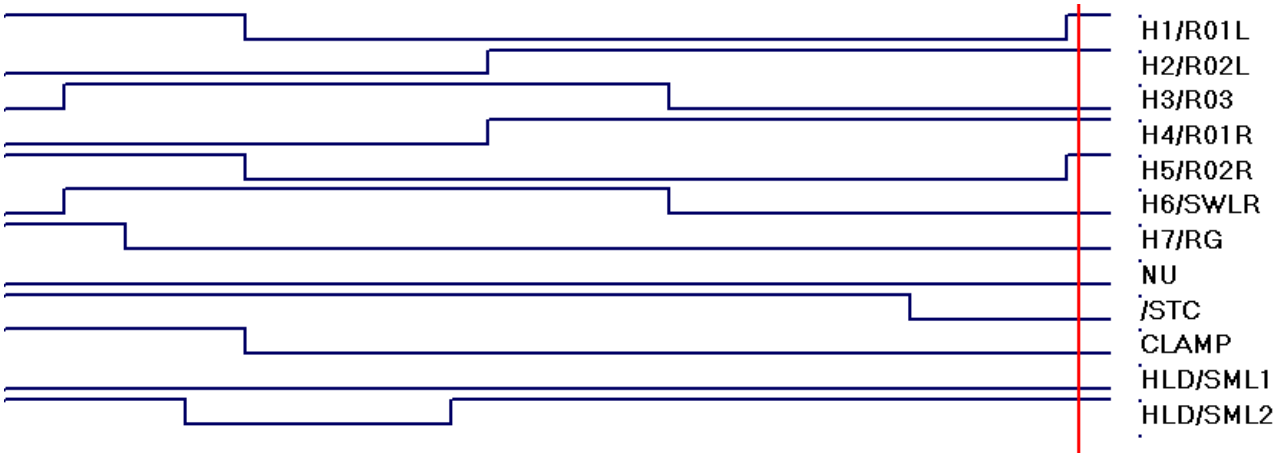


Figure 18 - horizontal readout Left

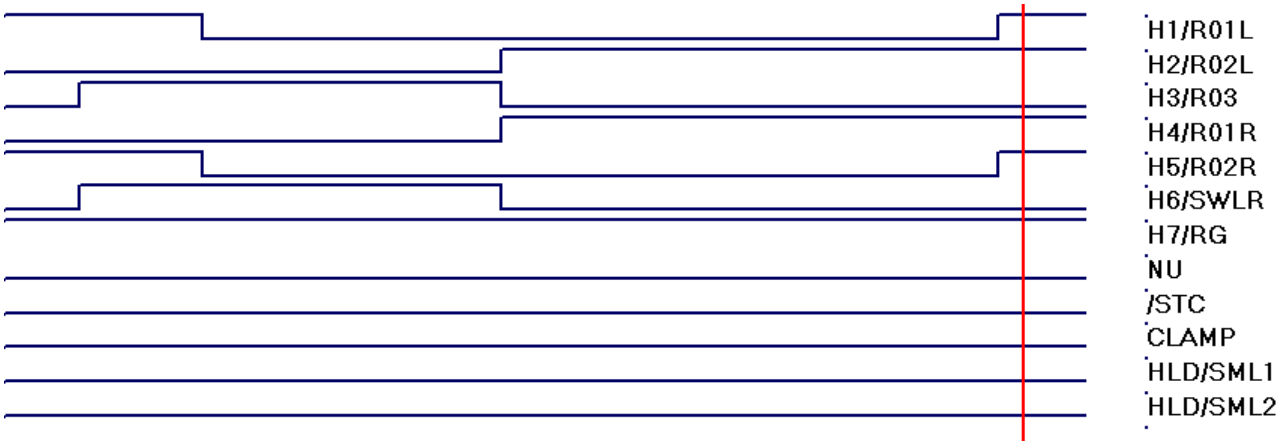


Figure 19 - horizontal skip Left

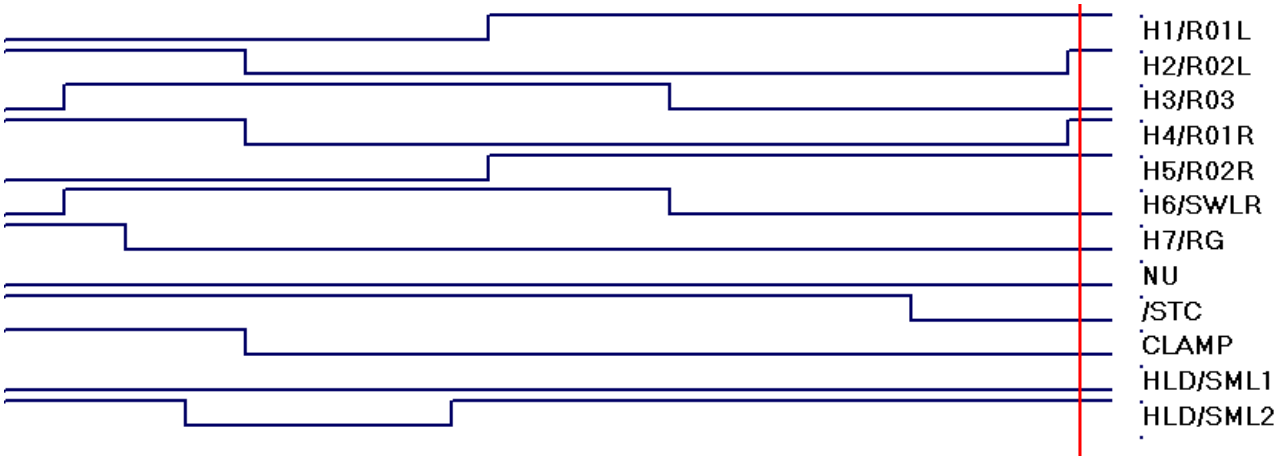


Figure 20 - Horizontal readout both

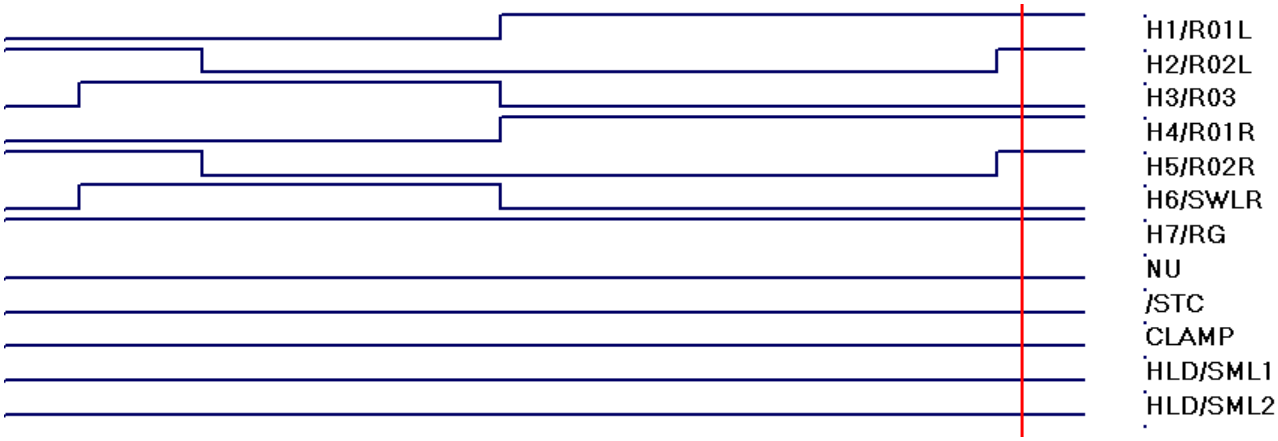


Figure 21 - horizontal skip Both

In the horizontal readout phases, the clamp signal is generated by an internal TTL signal (such as the STC and the HLDs signals). In the ARC controller we decide to use one of the clocks (DB 37, pin 11 = clock #10).

4.3 LRS phases generated by the Skytech CCD controller (oscilloscope)

From Figure 22 to Figure 25 are shown the real waveforms generated by the Sequencer and measured directly from the clock board.

These clock sequences are according to the foreseen phases and are used successfully by the LRS acquisition.

The goal is to generate the same phases with the ARC controller by modification of the assembler code provided by the Astronomical Research Controller Company.

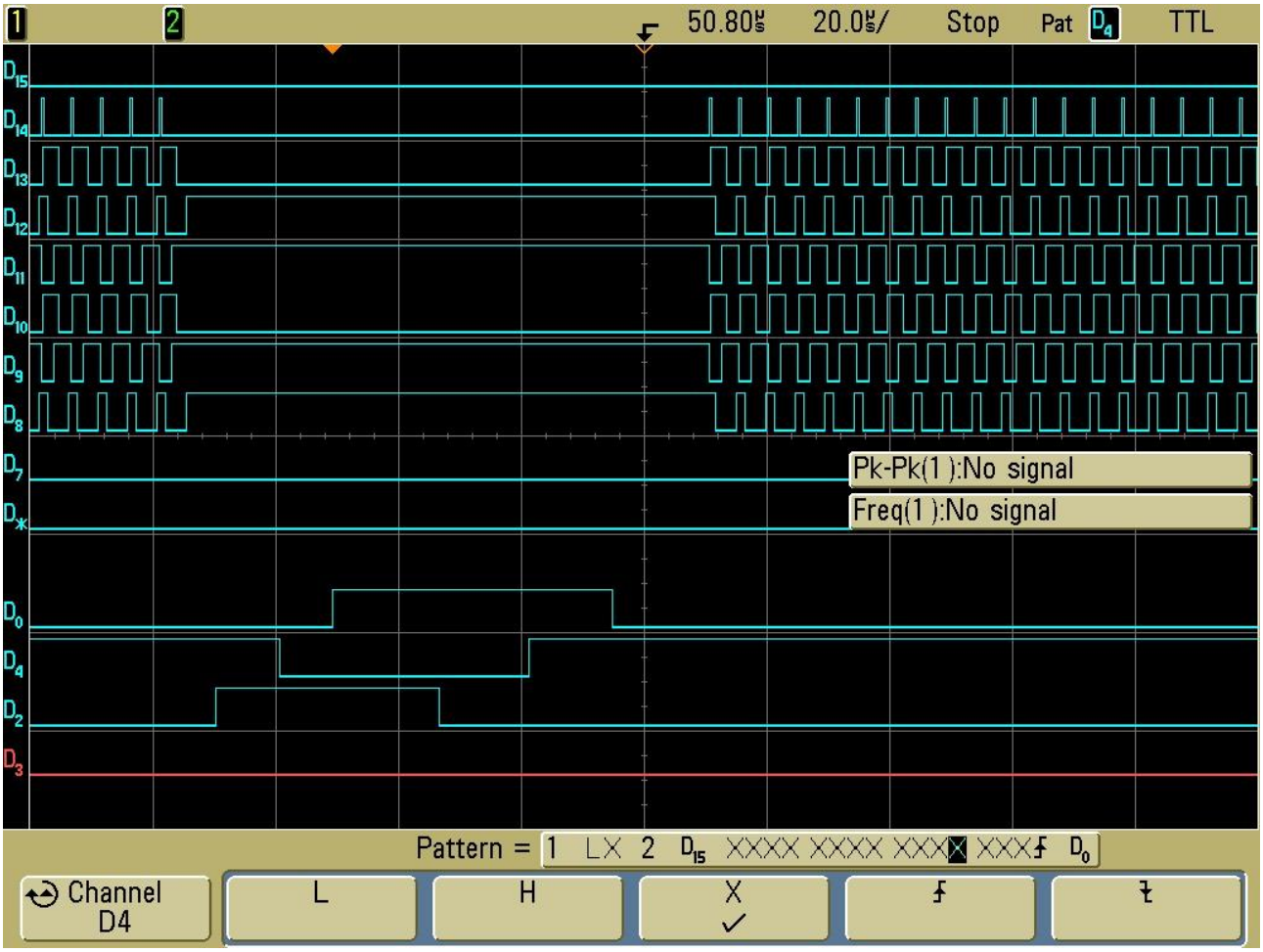


Figure 22 - Vertical and Horizontal clocks

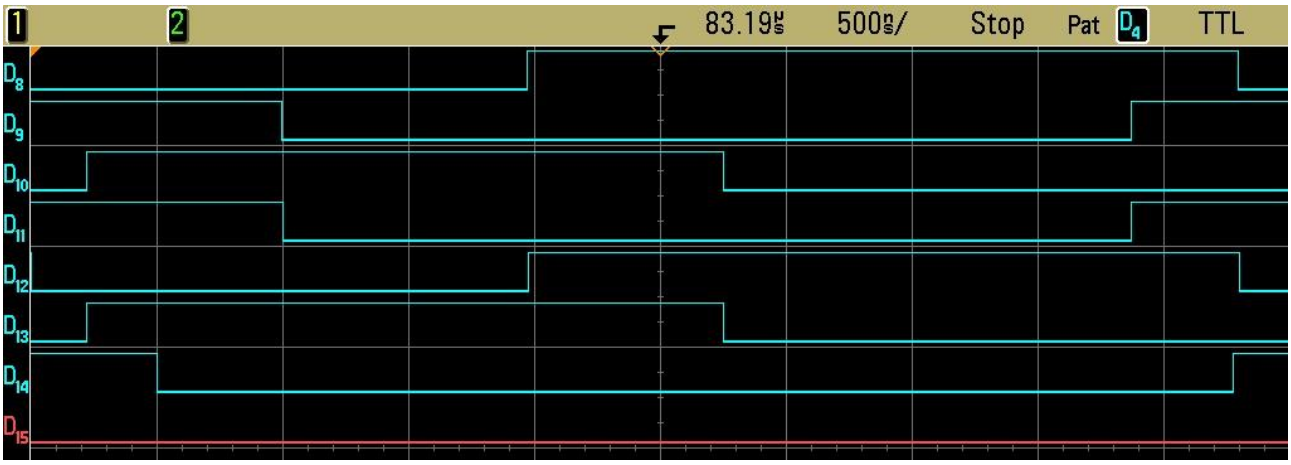


Figure 23 - Right readout

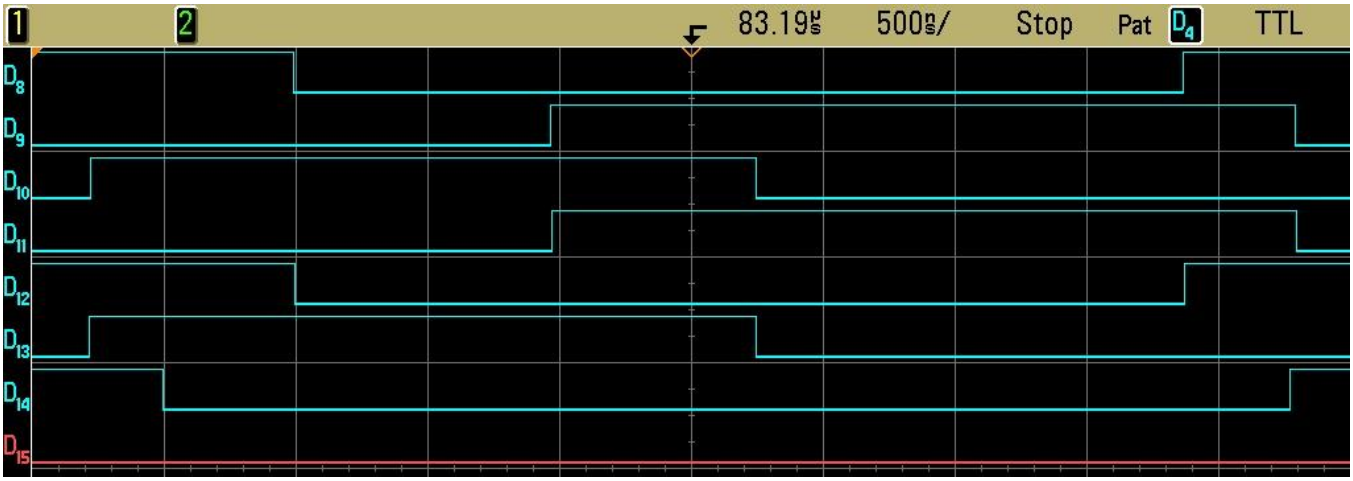


Figure 24 - Left readout

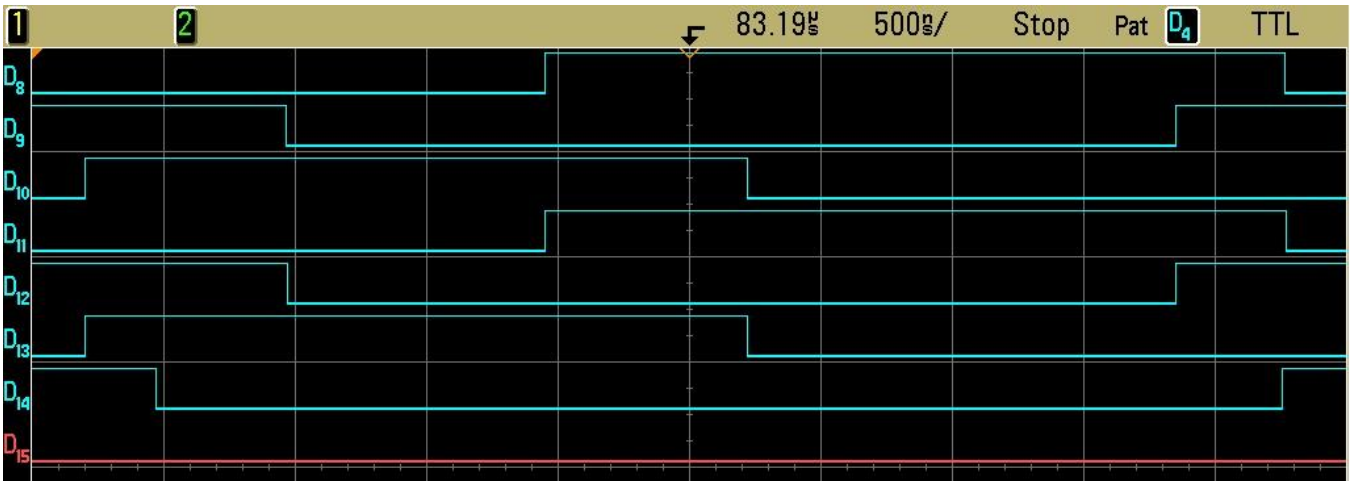


Figure 25 - Both readout

4.4 Clock configuration of the ARC controller

The configuration of the clock sequences in the ARC controller is be done changing the assembler code of the *.waveform file.

The code to change includes;

1. The assignment of the clock labels to the register
2. The settings of the clock ranges values
3. The setting of the sequences

4. Table 11 - Phases labels assignment

Clock register assignment			
RG	EQU	1	Reset Gate left, Pin 1
T0	EQU	2	test 0, Pin 2
H1L	EQU	4	Serial #1 left, Pin 3
H1R	EQU	8	Serial #1 right, Pin 4
H2L	EQU	$10	Serial #2 left, Pin 5
H2R	EQU	$20	Serial #2 right, Pin 6

H3	EQU	$40	Serial #3 both left and right, Pin 7
SW	EQU	$80	Summing well left, Pin 8
T1	EQU	$100	test 1, pin 9
T2	EQU	$400	test 2, pin 11
T3	EQU	$800	test 3, pin 12
I1	EQU	1	Image, phase #1, Pin 13
I2	EQU	2	Image, phase #2, Pin 14
I3	EQU	4	Image, phase #3, Pin 15
DG	EQU	8	Dump gate, Pin 16

Table 12 - Assembler register assignation (clocks range values)

CCD Clock values			
CL_HI	EQU	5	clamp max value
CL_LO	EQU	0	clamp min value
RG_HI	EQU	10.0	Reset Gate High
RG_LO	EQU	-2.0	Reset Gate Low
R_HI	EQU	9.0	Serial Register High
R_LO	EQU	-1.0	Serial Low
SW_HI	EQU	9.0	Summing Well High
SW_LO	EQU	-1.0	Summing Well Low
DG_HI	EQU	8.0	Dump Gate High
DG_LO	EQU	-2.0	Dump Gate Low
P_HI	EQU	8	Parallel High
P_LO	EQU	-2.0	Parallel Low
Vmax	EQU	13.0	Clock driver rail
ZERO	EQU	0.0	Unused pins
VODL	EQU	27.0	Output Drain Left
VODR	EQU	27.0	Output Drain Right
VRDL	EQU	15.0	Reset Drain Left
VRDR	EQU	15.0	Reset Drain Right
VOG1	EQU	1.0	Output Gate #1
VOG2	EQU	2.0	Output Gate #2
VSS	EQU	22.0	Substrate
VDD	EQU	24.0	Dump Drain
PWR	EQU	6.0	Preamp Power

DB 37 Clock	Clock #	register	E2V4240
1	clock 0	1	RG
2	clock 1	2	RG2
3	clock 2	4	H1L

4	clock 3	8	H1R
5	clock 4	$10	H2L
6	clock 5	$20	H2R
7	clock 6	$40	H3
8	clock 7	$80	SW
9	clock 8	$100	SWL
10	clock 9	$200	
11	clock 10	$400	**Clamp**
12	clock 11		
13	clock 12	1	I1
14	clock 13	2	I2
15	clock 14	4	I3
16	clock 15	8	DG
17	clock 16		
18	clock 17		
19	clock 18		
33	clock 19		
34	clock 20		
35	clock 21		
36	clock 22		
37	clock 23		

4.5 Bias configuration of the Skytech controller

[BIAS]
bias1=27.00
bias2=15.00
bias3=15.00
bias4=22.00
bias5=7.00
bias6=0.0
bias7=0.0
bias8=0.0
bias9=1.0
bias10=2.0
bias11=0
bias12=0
bias13=0
bias14=0
bias15=0
bias16=0

4.6 Bias configuration of the ARC controller

e2v 4240		Bias	Reference
VODL	EQU	27.0	Output Drain Left
VODR	EQU	27.0	Output Drain Right
VRDL	EQU	15.0	Reset Drain Left
VRDR	EQU	15.0	Reset Drain Right
VOG1	EQU	1.0	Output Gate #1
VOG2	EQU	2.0	Output Gate #2
VSS	EQU	22	Substrate
VDD	EQU	24.0	Dump Drain
PWR	EQU	6.0	Preamp Power

CCD		TNG		ARC	
Ref	Voltage	Bias	Voltage	Bias	Voltage
VOD	29	1	27		27
VRD	17	2	15		15
VRD	17	3	15		15
VDD	24	4	22		22
VSS	9.5	5	7		
		6	0		
		7	0		
		8	0		
VOG1	3	9	1		0
VOG2	4	10	2		1
		11	0		
		12	0		
		13	0		
		14	0		
		15	0		
		16	0		

Appendix A – Connectors and references

Table 13 - details of the connectors

	Connector	Qta	Serial		Use	code
ARC Connections	DB-15	1	RS-704-7441	ARC-board	ARC internal connections	FCE17-A15SM-240
	DB-25	1	RS-704-7466	ARC-board	ARC internal connections	FCE17-B25SM-240
	DB-37	1	RS-437-376	ARC-board	ARC internal connections	DC-37S-A191-A197
	MIL-16-26	1	RS-450-152	ARC-Panel	ARC internal connections	62GB-12E16-26SN
	MIL-20-41	1	RS-450-174	ARC-Panel	ARC internal connections	62GB-12E20-41SN
Cable Option 1	MIL-16-26	1	RS-450-310	ARC-Panel	cable ARC-Preamplifier	62GB-56T16-26PN
	MIL-CASE-26	1	RS-450-556	ARC-Panel	cable ARC-Preamplifier	62GB-585-16-26S
	MIL-20-41	1	RS-450-332	ARC-Panel	cable ARC-Clock	62GB-56T20-41PN
	MIL-CASE-41	1	RS-450-499	ARC-Panel	cable ARC-Clock	62GB-585-20-41P
	DB-44 FEMALE	1	RS-691-9048	Pre-box	cable ARC-Preamplifier	L77HDB44S
	DB-44 MALE	1	RS-691-9039	clk-box	cable ARC-Clock	L717HDB44P
	DB-44 CASE	2	RS-740-1245	clk-box		8655MHRA2501KLF
Cable Option 2	MIL-16-26	1	RS-450-310	ARC-Panel	cable ARC-cryostat video bias	62GB-56T16-26PN
	MIL-20-41	1	RS-450-332	ARC-Panel	cable ARC-cryostat clock	62GB-56T20-41PN
	MIL-CASE-41	1	RS-450-499	ARC-Panel	cable ARC-cryostat clock	62GB-585-20-41P
	MIL-16-26	2	RS-450-398	Cryostat	cable ARC-cryostat (Vid & CLK)	62GB-56T16-26SN
	MIL-CASE-26	3	RS-450-556	cable		62GB-585-16-26S
CCD	M83513	2	RS-719-5900	Cryostat-CCD	CCD-Connector 15pin	
	MWDM2L-21SS	2	RS-634-7305	Cryostat-CCD	CCD-Connector 21pin	
	MIL-16-26	3	Detoronics	Cryostat	Vacuum connectors	DT02H-16-26PN

Appendix B – Document identification code

ORG-TYP-INS-NCOD

ORG = Originator field (i.e. TNG)
TYP = Document Type (see Table 14)
PRJ = project element (see Table 15)
NCOD= numeric code (i.e. 0001)

Example: TNG-MAN-HAN-0001

Table 14 - Document type code

AD	Assumption Document
AN	AN Analysis
COS	Cost Documents (Estimate/CaC/CtC, etc)
DD	Design Description
DP	Data Package
DRD	Document Requirements Description/Definition
DRL	Document Requirements List
DW	Drawing/Diagram
EID	Experiment Interface Document
FI	File (Software/Configuration/Network)
ICD	Interface Control Document
IRD	Interface Requirement Document
ITT	Invitation to Tender
MAN	Manual/User Guide/Handbook
MEM	Memo
MOM	Minutes of Meeting
MOU	Agreement/Memorandum of Understanding
MX	Matrix/Compliance
NCR	Non-Conformance Report
NOT	Note
OPS	Operations Document
PLN	Plan

PO	Proposal
PRE	Progress Report/Status Report
RFQ	Request for Quotation
SOW	Statement of Work
TOR	Terms of Reference
TN	Technical Note
TP	Test Procedure/Test Plan
TR	Test Report/Test Result
TS	Test Specification
VC	Verification Control Document
WBS	Work Breakdown Structure
WP	Working Paper
WPD	Work Package Description

Appendix C – Project Element Code

Table 15 – Project element code

BTM	Batman
CCD	CCD detector/electronic/software
HAN	HARPSN
TRK	Tracking
DOL	Dolores
SRG	SARG

Appendix D – List of Acronyms

ARC	astronomical research camera
BOM	Bill Of Material
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
EMC	electromagnetic compatibility
EMI	Electromagnetic Interference
INAF	Istituto Nazionale di AstroFisica
LRS	Low Relolution Spectrograph (Dolores)
TBC	To Be Confirmed
TBD	To Be defined
TBF	To be fixed
TNG	Telescopio Nazionale Galileo
TTL	transistor-transistor logic